Parallelized FMM and Dedicated PEEC Method to Model Industrial Power Interconnections – Application to Boost Chopper

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Abstract — This paper presents a novel version of a dedicated PEEC-based (Partial Element Equivalent Circuit) methodology applied to the modeling of interconnections of power electronics devices. Although this method is known, the originality of this work is its use to quickly model structures presenting an industrial complexity thanks to two separated and now parallelized Fast Multipole Methods (FMM) based on two different meshes. They respectively compute parasitic inductances and capacitances and lead to an equivalent circuit of the system. EMC performances of a structure can be evaluated with time and frequency domain analysis of this circuit. This approach is applied to model two static converters, boost choppers built with routing parts of an industrial variable speed drive.

I. INTRODUCTION

Since several years, power interconnections and consequently EMC modeling of industrial static converters are real challenges because of the frequency rise, the growing complexity of components, the closed environments and the strong electromagnetic couplings. The PEEC method based on integral equations appears to be efficient to model interconnections of large VLSI structures [1]. However its use in power electronics needs some adaptations in order to get non-large models because EMC standards are focused on frequencies ranging from 10 kHz to 200 MHz. That was the purpose of our previous works [2] in which inductive and capacitive models were separately dealt with. Thus, it was possible to take advantage of both approaches and especially of the different meshes and hypothesis to extract equivalent elements that were finally coupled in a complete lumped element circuit.

The purpose of this article is to present some interesting improvements as a matter of time and memory consumption in the extraction of parasitic elements: the use of FMM algorithm [3] is generalized to the computation of inductances (L) and mutual-inductances (M) and secondly the parallelization of algorithms is applied during the integration, preconditioning and solving process. These enhancements make it possible to quickly process even larger industrial structures with few memory consuming.

In the second part of the article, the adapted PEEC approach is reminded and its improvements are detailed, with some numerical results on speed-up factors. The methodology is then applied to model a boost chopper, composing the industrial variable speed drive already modeled in [2]. New results, in frequency and time domains, obtained thanks to the improved techniques are finally presented in the last part of the paper.

II. EXTRACTION OF (R-L-M-C) EQUIVALENT CIRCUIT

A. Two separated FMM and preconditioned GMRES(m)

In our approach [2] a dedicated inductive mesh is used to compute parasitic equivalent resistances and inductances (R-L-M) by a full integral method and a second discretization is needed for the FMM-based capacitances (C) calculation. These two meshes are respectively adapted to skin depth and side effects to precisely model the current and surface charge distributions.

The use of FMM is now generalized for the inductive part in order to accelerate the computation of the vector magnetic potential **A**: a new multipole $\mathbf{M}_n^m$ is computed from the same spherical harmonics Y_n^m and scalar free-charges in [2] are replaced by current density vector **J** (1).

$$\begin{cases} \mathbf{A}(\rho,\theta,\varphi) = \dfrac{1}{4\pi\varepsilon_0}\displaystyle\sum_{n=0}^{\infty}\sum_{m=-n}^{n}\mathbf{M}_n^m.Y_n^m(\theta,\varphi)/\rho^{n+1} \\ \mathbf{M}_n^m = \displaystyle\sum_{i=1}^{Nq}\mathbf{J}_i r_i^n Y_n^{-m}(\alpha_i,\beta_i) \end{cases} \quad (1)$$

Since the "inductive" and "capacitive" multipoles are respectively vectors and scalars, the use of two different cube partitionings for the two meshes and two different iterative solvers is required. A preconditioned GMRES(m) [4] algorithm is also used to solve the current distribution or the (R-L-M) inductive components.

As an example proving the computation enhancements, a 1.6 Gbytes of memory inductive problem solved without FMM can be now solved with only 230 Mbytes and five times faster (100 s). Another structure (induction heating device) has been simulated by FMM with 11 Gbytes of memory instead of more than 405 Gbytes without FMM.

B. Parallelization of algorithms

To take advantage of widespread multi-core computers, most algorithms have been parallelized, i.e. the computation of Gauss point tables, the integration of small full matrixes, the computation of scalar and vector potential V and **A**, the two GMRES(m) preconditioning processes, the matrix-vector products during the GMRES(m) solving, etc.

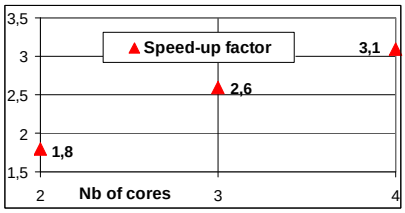

Fig. 1. Average performances of all parallelized algorithms

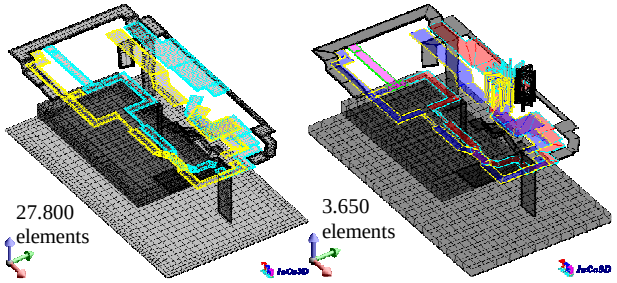

Fig. 2. Capacitive (left) and inductive (right) meshes - InCa3D [5]

The average speed-up factors of all parallelized algorithms are shown in Fig.1: for example, with two cores, the parallelized process time is divided by 1.8. The gap with the ideal factor of two is due to the increase of data exchanges between the processors.

III. Application to Boost Chopper

All these methods are applied to model a boost chopper in two different configurations: the interconnections are routed on two or four copper layers. The device is composed by the mechanical part and two of the three phases of the industrial variable speed drive presented in [2].

A view of the capacitive and inductive meshes is given in Fig.2. The extraction of inductive and capacitive equivalent parasitic elements is done by the two FMM and GMRES(m) algorithms. 35 and 40 capacitive regions are defined for the two prototypes and one parasitic capacitance is automatically connected between each pair of regions; the connection points depend on the distance between each region. Thus, a complete equivalent RLMC circuit is built and an equivalent impedance representation of it could possibly be exported to a circuit simulator.

In our study, the impedance spectrum of the two prototypes is firstly analyzed with the expedient of replacing all the electrical components (diode, transistor, inductances, etc.) by a short circuit, in order to focus on the parasitic RLMC behavior. This analysis points the different capacitive behavior of the routings, in fact the first frequency resonance of the two and four-layer structures appears at 58 MHz and 36 MHz, respectively.

Time-domain simulations of the whole model in a circuit solver and measurement comparisons have then validated the electrical functioning of the two structures and consequently our model. The influence of interconnections during the switching can be pointed out. EMC performances can be easily investigated. For example the common mode voltage at the terminal of the LSIN resistance is plotted for

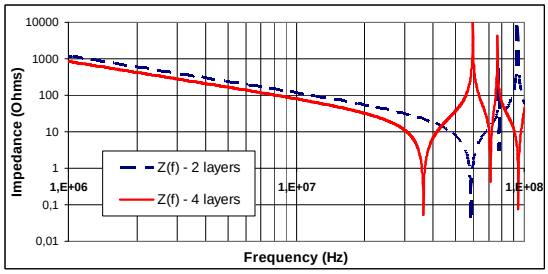

Fig. 3. Impedance spectrum of the two prototypes (1-100MHz)

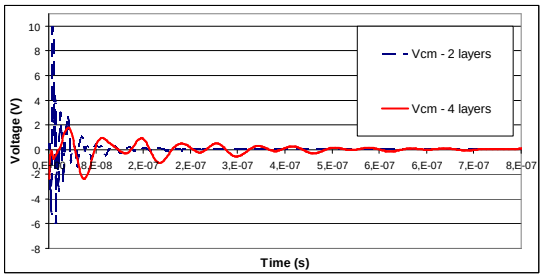

Fig. 4. Common mode voltage during the transistor switching

the two prototypes in the figure 4. The prototype composed of four layers produces less common mode voltage than the other structure. In this last analysis, the minimum time step is 0.1 ns. One period of 65.5 µs is simulated in 4 minutes in the circuit solver Portunus [6].

In the extended paper, more details on these simulations and comparisons with measurements will be given.

IV. Conclusions

In this paper, a novel version of a dedicated PEEC method of industrial power interconnections is presented. Like for the capacitive modeling, the use of FMM and GMRES(m) algorithms for the inductive part makes possible to deal with larger structures with few memory consumption. Also the parallelization of most of algorithms further improves the time process.

Thus it is possible to quickly obtain small interconnection models of industrial complexity which include the main magnetic and electrical couplings. To finish, EMC performances of a complex device is evaluated in a circuit solver thanks to this approach.

V. References

[1] A. E. Ruehli, “Survey of computer-aided electrical analysis of integrated circuit interconnections,” IBM J. Res. Develop., vol. 23, pp. 626–639, Nov. 1979.

[2] V. Ardon, J. Aimé, O. Chadebec, E. Clavel, J.- M. Guichon, E. Vialardi, “EMC Modeling of an Industrial Variable Speed Drive with an Adapted PEEC Method”, IEEE Transactions on Magnetics, Vol. 46, N°8, Aug 2010.

[3] J. Carrier, L. Greengard, and V. Rokhlin, “A fast adaptive multipole algorithm for particle simulations, SIAM J. Sci. Statist. Comput., 1988.

[4] Y. Saad and M. H. Schultz, “GMRES: A generalized minimal residual algorithm for solving nonsymmetric linear systems,’’ SIAM J. Scientific and Statistical Computing, vol. 7, pp. 856-869, July 1986

[5] InCa3D software, Cedrat, www.cedrat.com

[6] Portunus software, Adapted-Solutions, www.adapted-solutions